WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a first die having:

a substrate with an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having:

a micro-electromechanical structure having an inductance;

a plurality of third bonding pads connected to the micro-electromechanical structure; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

2. The integrated circuit of claim 1 and further comprising:

a semiconductor package, the semiconductor package having a plurality of fourth bonding pads, a plurality of circuit board connectors, and internal routing that electrically connects the plurality of fourth bonding pads to the plurality of circuit board connectors, the first die being attached to the semiconductor package; and

a plurality of wires connected to the first bonding pads and the fourth bonding pads.

3. The integrated circuit of claim 1 wherein the second die further includes a micro-electromechanical structure that has a capacitance.

4. A method of forming an integrated circuit, the method comprising the steps of:

forming a first die from a first wafer, the first die having:

a substrate with an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect; and

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

forming a second die from a second wafer, the second die having:

a micro-electromechanical structure having an inductance; and

a plurality of third bonding pads connected to the micro-electromechanical structure; and

attaching the third bonding pads of the second die to the second bonding pads of the first die.

5. The method of claim 4 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps and the second

die is fabricated at a second facility using a different second sequence of fabrication steps.

6. The method of claim 4 wherein the first die is fabricated at a facility using a first sequence of fabrication steps and the second die is fabricated at the facility using a different second sequence of fabrication steps.

7. The method of claim 4 wherein the third bonding pads of the second die are attached to the second bonding pads of the first die at the first facility.

8. The method of claim 4 wherein the third bonding pads of the second die are attached to the second bonding pads of the first die at the second facility.

9. The method of claim 4 wherein the third bonding pads of the second die are attached to the second bonding pads of the first die at a third facility.

10. The method of claim 4 and further comprising the step of attaching the first die to a semiconductor package, the semiconductor package having a plurality of fourth bonding pads, a plurality of circuit board connectors, and internal routing that electrically connects the plurality of fourth bonding pads to the plurality of circuit board connectors.

11. The method of claim 10 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second

die is fabricated at a second facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at a third facility, and the first die is attached to the semiconductor package at the third facility.

12. The method of claim 10 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second die is fabricated at a second facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at a third facility, and the first die is attached to the semiconductor package at a fourth facility.

13. The method of claim 10 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second die is fabricated at a second facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at the first facility, and the first die is attached to the semiconductor package at the first facility.

14. The method of claim 10 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second die is fabricated at a second facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at the second facility, and the first die is attached to the semiconductor package at the second facility.

15. The method of claim 10 wherein the first die is fabricated at a facility using a first sequence of fabrication steps, the second die is fabricated at the facility using a different second sequence of fabrication

steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at the facility, and the first die is attached to the semiconductor package at the facility.

16. The method of claim 10 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second die is fabricated at the first facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at a second facility, and the first die is attached to the semiconductor package at the second facility.

17. The method of claim 10 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second die is fabricated at the first facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at a second facility, and the first die is attached to the semiconductor package at a third facility.

18. The method of claim 10 and further comprising the step of attaching a plurality of conductive wires to the plurality of first bonding pads and the plurality of fourth bonding pads.

19. The method of claim 18 wherein the first die is fabricated at a first facility using a first sequence of fabrication steps, the second die is fabricated at a second facility using a different second sequence of fabrication steps, the third bonding pads of the second die are attached to the second bonding pads of the first die at a third facility, the first die is attached to the semiconductor package at a fourth facility, and the plurality of conductive wires are attached in the fourth facility.

20. The method of claim 4 wherein the second die further includes a micro-electromechanical structure that has a capacitance.

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